EMPIR – 14IND07 3DStack

Guide for conformity assessment for electrical and thermal properties of TSVs

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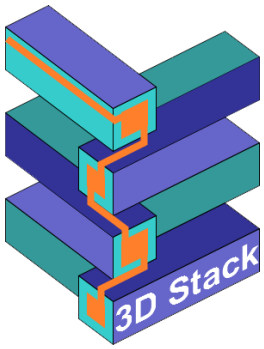
Abstract: *This document gives overview of the measurement techniques dealing with electrical and thermal properties both at wafer level (based on specialized test structures) and at individual TSV level (individual TSVs or cross-sections). Main aim of this guide is to quantify the role of measurement uncertainty for electrical resistivity of TSVs, thermal dissipation around TSVs and thermal conductivity and to give guidance for making electrical and thermal properties on TSVs traceable.*



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1. Introduction

1.1 Motivation

There are various electrical and thermal characteristics that can be studied on TSVs and numerous experimental techniques that can be used for it. In this guide, we present a list of major experimental techniques and related measured quantities, divided into two main groups. First, methods that are based on specific test structures prepared at manufacturing stage are described. The goal of such test structures is to create a statistically relevant set of results and to be able to do automated tests during various technological steps during its manufacturing. Second, methods that are addressing individual TSVs (either on real world samples or on artificially prepared structures) are discussed. These are more research focused techniques, trying to answer questions of what affects electrical or thermal properties of particular TSV, e.g. what is the role of fill material defects on the resistivity.

The typical connection scheme of a TSV is illustrated in Fig. 1. The TSV consists of a vertical cylindric conductor, crossing the silicon substrate and enabling the electrical connection between the front side (usually METAL1) and the backside metallization (or redistribution layer, RDL) in a thinned wafer. The TSV conductor is electrically insulated from the silicon substrate by a dielectric layer (TSV Insulator in Fig. 1), usually SiO_2, ~ 100-200 nm thick, conformally deposited after etching the TSV hole in the silicon. A thin barrier layer, a few nm thick, is deposited between the insulator and the conductor to prevent Cu diffusion in the Si oxide.

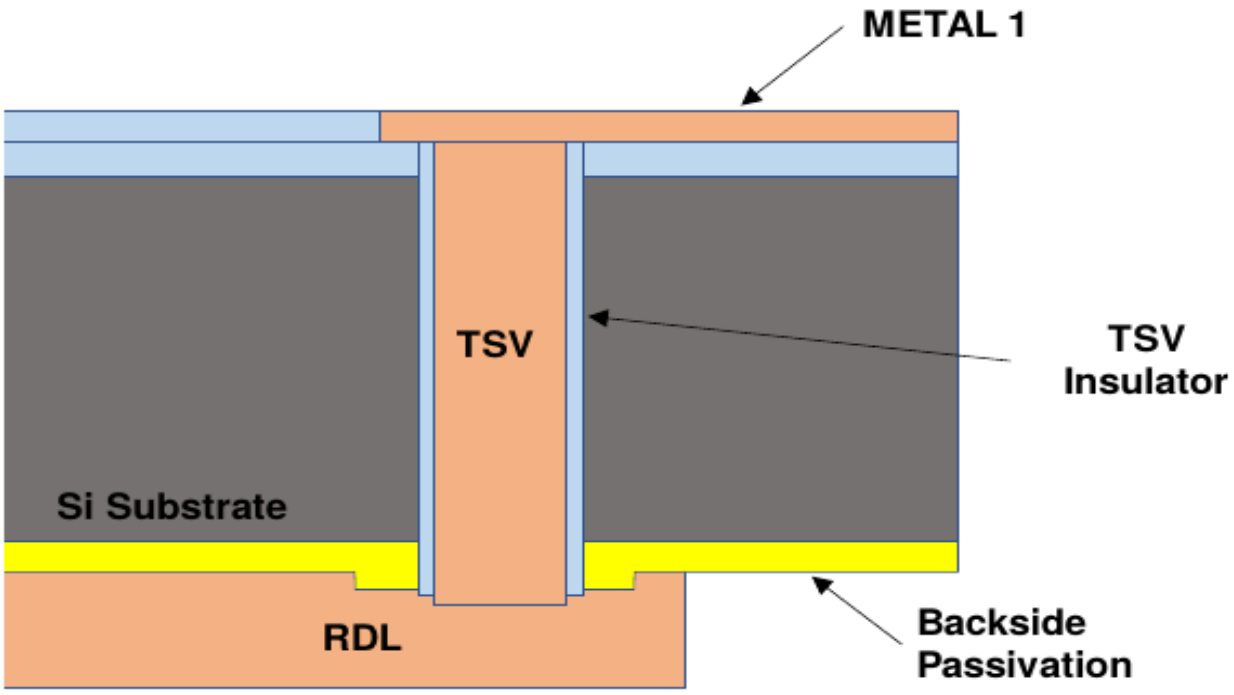


Figure 1: Schematic representation of a TSV cross-section, showing the TSV conductor connecting the lower interconnect level at the front side to the backside metallization, RDL, of a thinned wafer.

1.2. Industrial requirements on the quality characteristics

Measurement uncertainty for the electrical measurements is discussed as follows, however the situation is quite complex as requirements of TSVs properties are application dependent. There are as many TSV specifications as kinds of TSVs (first, middle, last…). In general, we would recommend that the accuracy is one or two orders of magnitudes better than what the expectation values are. That means that if the TSV resistance is typically in the range of a few mOhm, than, 0.1 mOhm to 0.01 mOhm accuracy should be sufficient for most of the applications.

As **example** we can take 10x100 µm TSV done at CEA-Leti with following quality characteristics:
- Kelvin structures measurement specification are following: target ~30 mOhms per TSV (+/- 5 mOhms). Resistivity was measured by 4 probes method.
- Capacitance measurement : typically ~1 picoFarad (probe at high frequency).
- No thermal effect found for this type of TSV (low power).

In fact, the main challenge for this sample comes from mechanical constraints inducing electron mobility variation (defining the keep out zone). Industrial partners usually adapt their request and design as a function of sample results and specifications.

Furthermore, some questioning and limitations that should be considered follows:
- One limitation we have today is that electrical/thermal simulations are usually based on 2D structures and we assume that these simulation results are 3D valid. This is also important if we want to use simulations for rough estimation of uncertainties.
- Moreover, there is still questioning about TSV aging and impact on the surrounding (Cu migration and related phenomena).
- Finally, there are strong needs to characterize the seed barrier around the TSV (isolation), shape, roughness, etc.

For information, please check following references [1,2] with more info about electrical tests done on 10x80 µm and 10x120 µm TSVs.

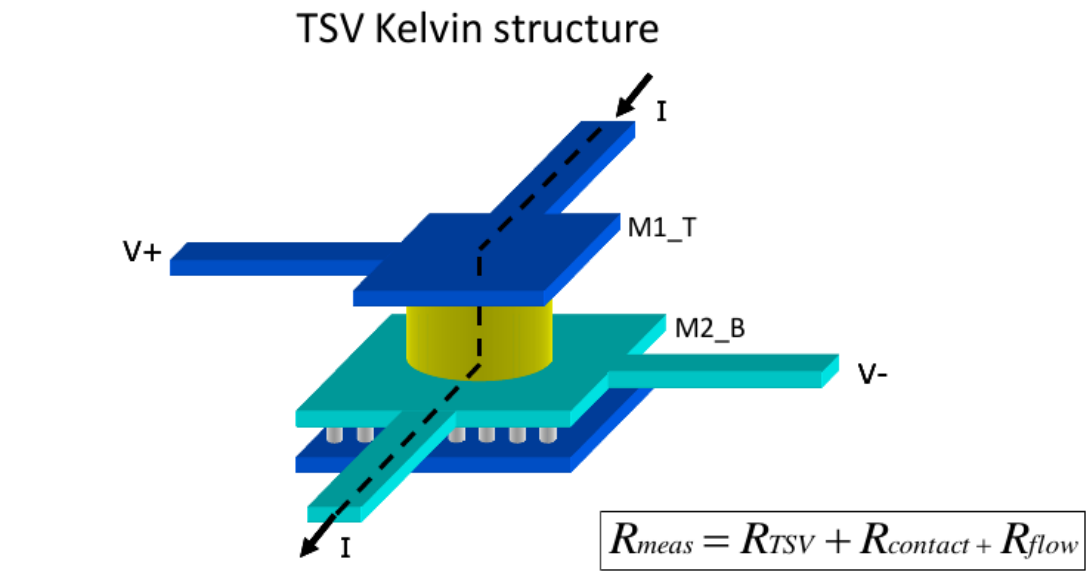
2. Methods for TSVs testing at wafer level, quality characteristics

Four types of measurements are discussed for the TSV characterization: Resistance, continuity yield, capacitance, leakage current. For TSV reliability, the liner/barrier assessment is an essential aspect to verify. In this context, the controlled *I-V* technique is discussed and proposed as an alternative to the traditional TDDB characterization.

2.1. TSV resistance

The section of the TSV conductor, usually Cu, is relatively large when compared to 2D on-chip interconnects. The TSV diameter, *D*, considered in these guidelines ranges from 5 □m down to 500 nm, according to the 3D integration strategy and to the 3D application. The TSV aspect ratio, *AR*, defined as TSV diameter/length, is usually in the 1-10 range, which enables a good conformality of insulator and barrier layers deposition, and a complete metal filling of the TSV conductor core. The corresponding TSV length *L* is between 500 nm (*D* = 500 nm) and 50 □m (*D* = 5 □m). With these dimensions, assuming a Cu resistivity = 22 mOhm*□m and by neglecting the insulator thickness which

takes away some area to the conductor, the theoretical minimum TSV resistance is ~60 mOhm.
To measure such a small resistance, the test structure requires a 4-point Kelvin configuration of the TSV, as illustrated in Fig. 2. This configuration prevents the measured TSV resistance to be affected by the contact resistance of the probes on the measurement pads.



$$R_{meas} = \frac{V^+ - V^-}{I}$$

$R_{contact}$ = contact resistance of Cu nail with landing pad

R_{flow} = resistance due to change of current direction (Horiz. - Vert. - Horiz.) in the TSV

R_{via} = resistance of the vias between M1 and M2 in the stacked dies

Figure 2: Schematic of the 4-point test structure for measuring the resistance of a single TSV.

Different resistance contributions can be identified in the measured TSV resistance: the resistance of the TSV conductor, the contact resistance of the TSV with the landing pad, and the resistance due to the current crowding at the edges of the structures. In an optimized TSV manufacturing process, the last two contributions are usually negligible with respect to the first one. Fig. 3 shows a typical cumulative plot of the measured resistance of TSV Kelvin structures.

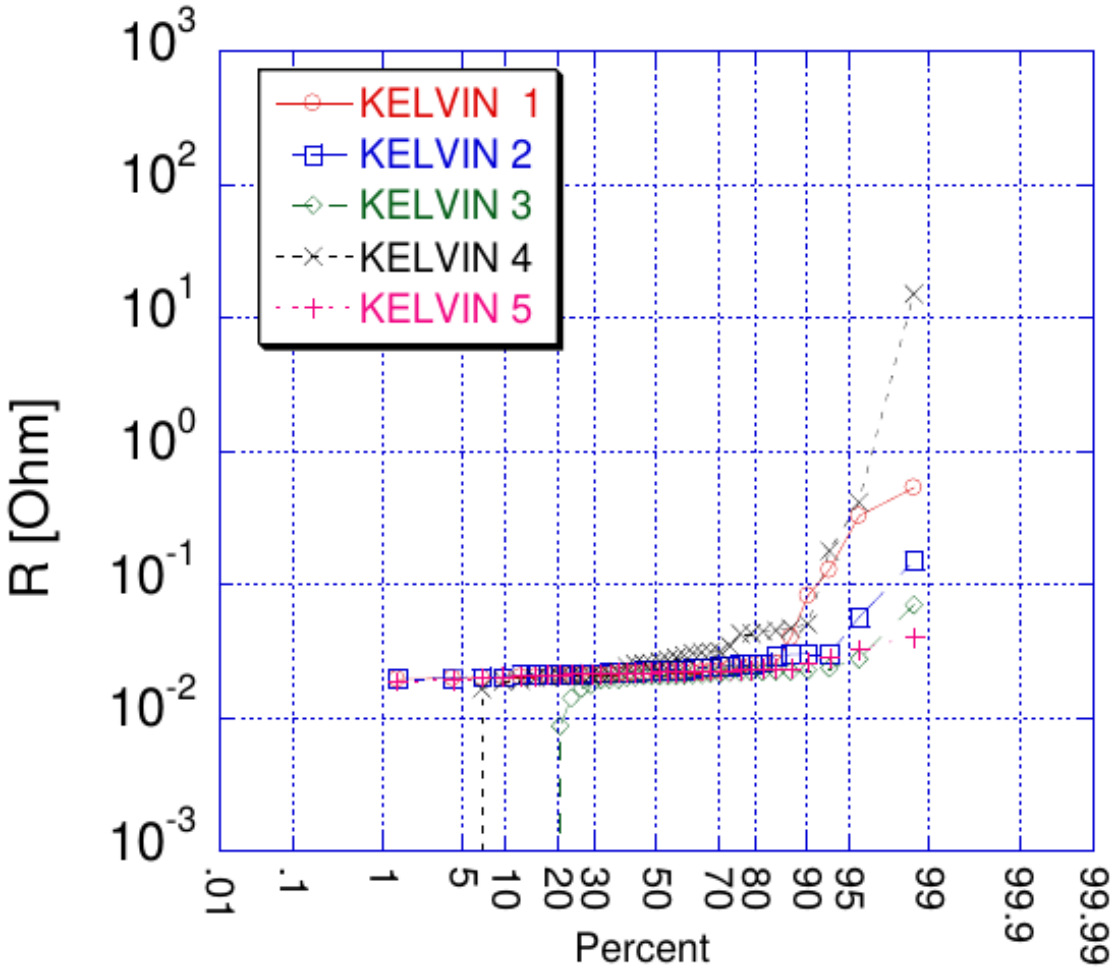


Figure 3: Cumulative plot of the TSV resistance measured on five Kelvin structures per die in 35 dies in the same wafer.

The low resistance measurement in the 10 mOhm range imposes some requirements in the measurement equipment. The capability in current should be in the 100 mA range for generating a voltage drop of 1 mV.

2.2 TSV continuity yield

The TSVs should provide a low resistance connection in all the locations of the same die where it is present. This yield requirement can be assessed with a TSV chain, consisting of many TSVs connected in series, Fig. 4.

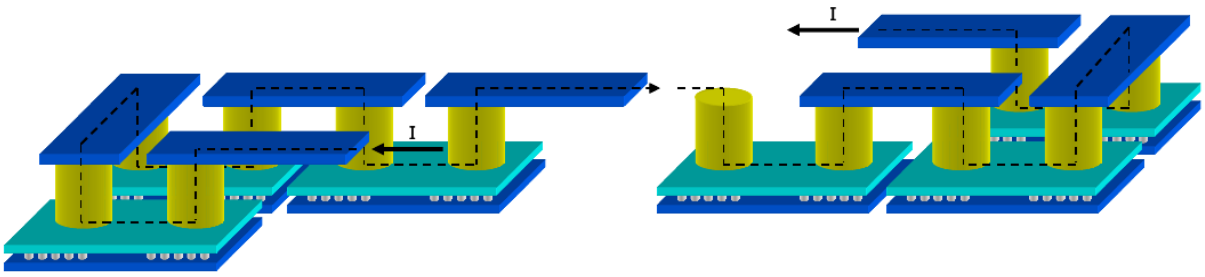


Figure 4: TSV chain concept: the chain continuity depends on the continuity of each single TSV in it.

The electrical continuity of the chain occurs if all the TSVs in it provide electrical connection. Typical numbers of TSVs in a chain may range from 100 to 1 M, leading to resistance values between 10 Ohm and 100 kOhm. The chain can be designed to allow measuring intermediate groups of subsequent TSVs, see Fig. 5.

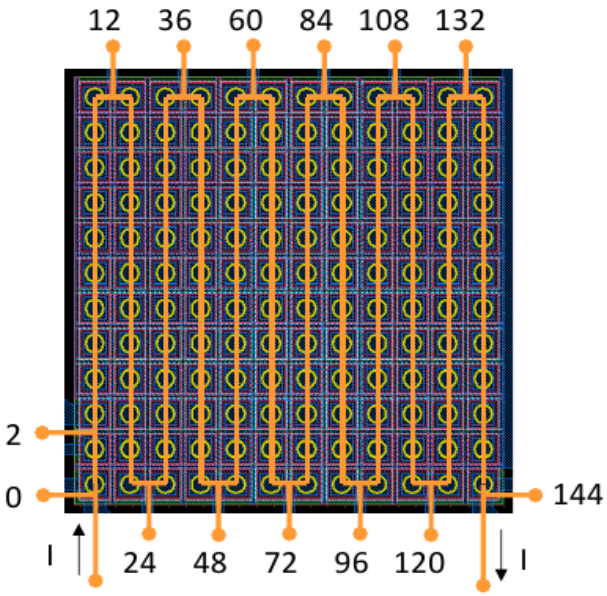


Figure 5: Layout of a TSV chain with the possibility to measure different groups of TSVs, by providing intermediate connections. Numbers indicate how many TSVs are included in each group, starting from the 0 terminal.

This option facilitates the search of a faulty TSV by allowing the identification of a smaller part of the chain where the open occurs, with respect to the entire chain. The granularity of the location depends on the number of TSVs in each part, defined during the design of the chain. The chain resistance may range from few Ohms to hundreds of kOhm, according to the number of TSVs in it; the use of a 4-point or a 2-point measurement configuration is chosen accordingly. By dividing the chain resistance by the total number of TSVs in it, the resistance of a TSV link can be extracted. The TSV link includes part of the metal segments connecting the TSVs in series, as shown in Fig. 6; therefore, its resistance is always higher than the TSV resistance of the single kelvin structure described in the previous section. Typical cumulative plot of the resistance of TSV chain structures is presented in Fig. 7.

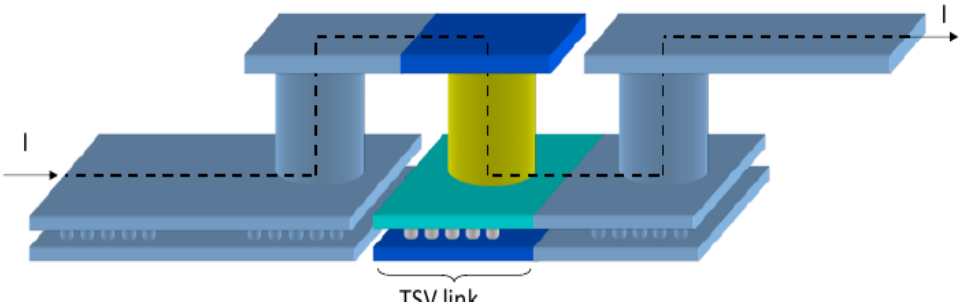


Figure 6: The resistance of a TSV link in a TSV chain can be extracted by dividing the measured resistance by the number of TSVs in the chain. This resistance includes the TSV resistance plus the contribution of the top and bottom metals connected to the TSV in the link.

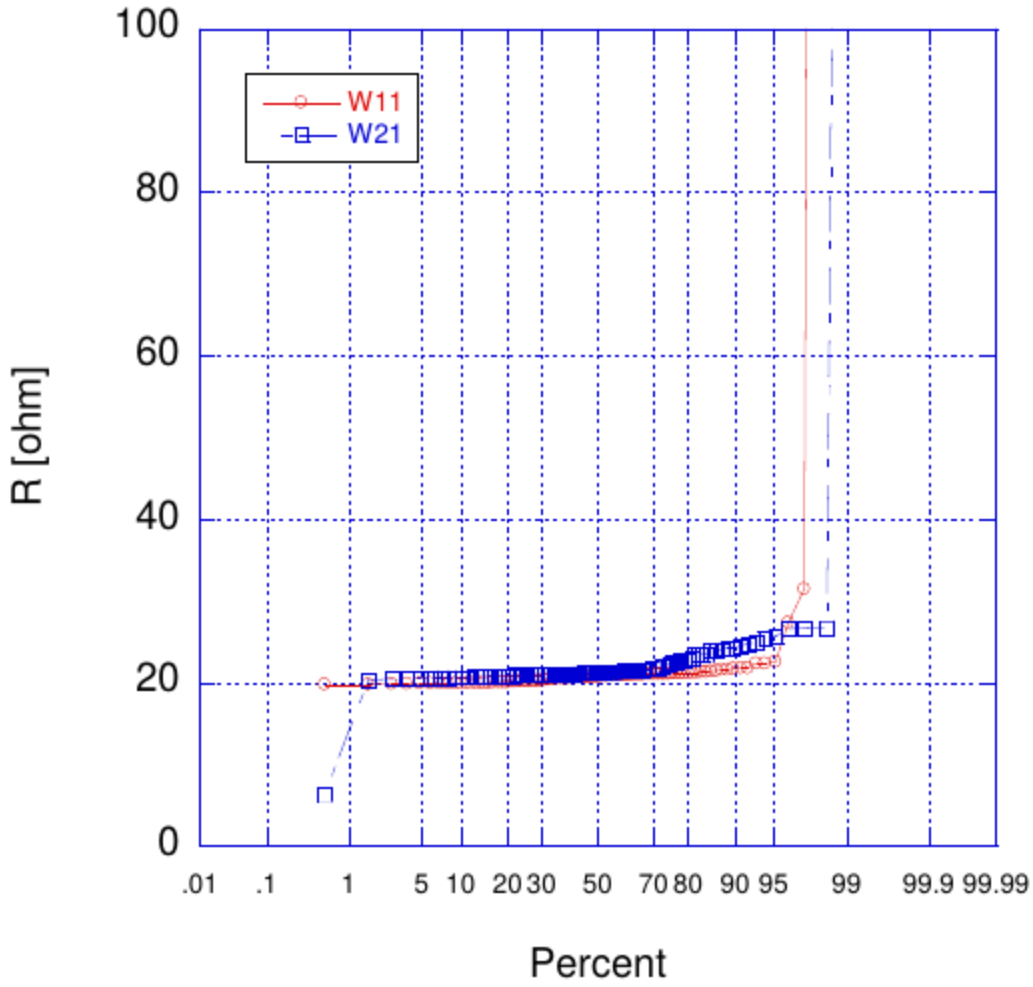


Figure 7: Cumulative plot of the TSV chain resistance measured on 92 dies in two different wafers.

The requirements of the measurement equipment are less stringent with respect to the single TSV kelvin, due to the larger values of resistance expected from the chain. 10 □A current is sufficient to generate a 1 mV voltage drop on a 100 Ohm chain resistance.

2.3. TSV capacitance

By assuming an insulator thickness *thk* = 200 nm, with a relative dielectric constant *k* = 4.4 (Si oxide), the calculated TSV capacitance in accumulation is ~125 fF for *D* = 5 □m and *L* = 50 □m; for *thk* = 20 nm, *D* = 500 nm and *L* = 500 nm, the TSV capacitance is around 1 fF.
The TSV capacitance can be measured by an impedance or LCR meter, connected to probe-stations for wafer-level measurements. The frequency range of the measurement is typically 10 kHz – 100 kHz. Accurate measurements require DUT capacitances of at least 1 pF, in any case larger than the parasitic capacitances of the probe-station and relative cables. Given the small capacitance of a single TSV, a sufficiently large capacitance can be obtained by more TSVs connected in parallel. The TSV capacitor test structure is therefore designed as an array of TSVs, interconnected by a metal network and accessible by a single terminal; a p+ substrate contact (in case of p-type substrate) is provided as the

second terminal of the TSV capacitor. The TSV array is repeated several times in the layout with the same interconnect network, but with a different number of TSVs inside; one array can be even available without any TSV. This structure is illustrated in Fig. 8 with four arrays with a different number of TSVs per each of the three available pitches.

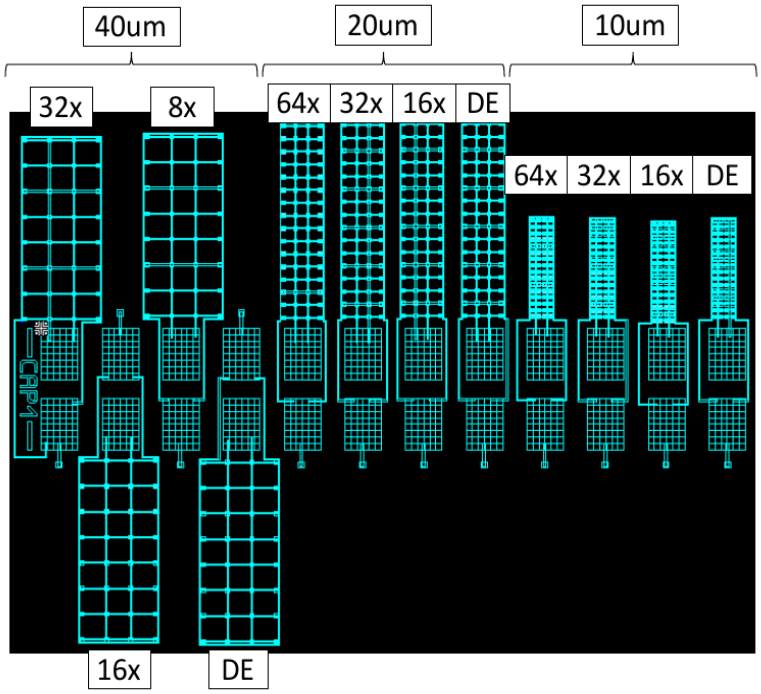


*Figure 8: Example of TSV arrays with different pitches (10, 20, 40 □*m*) and TSVs with D = 5 □*m*, L = 50 □*m *and thk = 200* nm*. The same TSV array contains different numbers of TSVs for each pitch; the DE array contains 0 TSVs.*

The min. number of TSVs in the array is set to reach a capacitance higher than 1 pF. All the arrays with different numbers of TSVs are measured in accumulation. The measurement results of the arrays in Fig. 8 are plotted in function of the number of TSVs in Fig. 9, per each pitch. The slope of the linear fitting of the measured values provides the capacitance of a single TSV, which in this example is about 127 fF; the intercept with the *Y* axis represents the parasitic capacitance of the interconnect network, which is common by designs to all the arrays with different numbers of TSVs. This value, indicated with DE, is consistent with the value measured on the array without TSVs.
The same structure can be used for C-V measurements, where both the accumulation and depletion values of the TSV capacitance can be characterized.

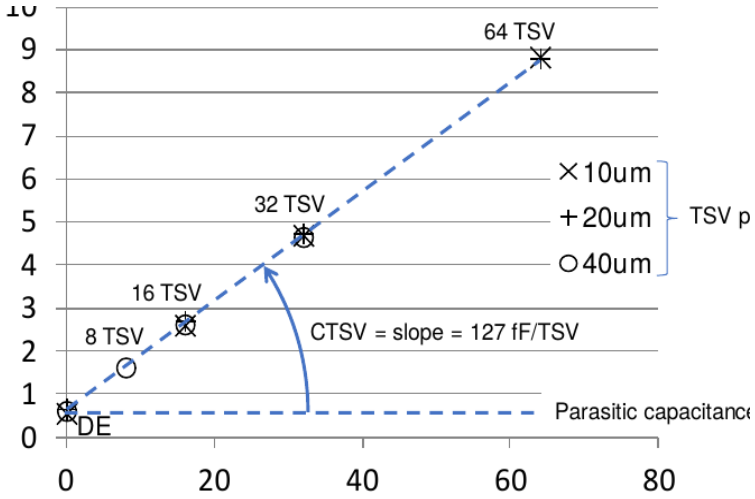


Figure 9: Measurement results on the TSV arrays in Fig. 8. All the values show a good linear progression with the number of TSVs, with no dependence on the TSV pitch. The intercept of the linear fitting with the Y axes (#TSV=0) provides the parasitic capacitance due to the interconnect network, which is consistent with the values measured on the DE structures without TSVs.

2.4. TSV leakage

The isolation of the TSV conductor from the substrate can be assessed by *I-V* measurements between the TSV conductor and the Si substrate. A suitable test structure is the TSV array capacitor described in the previous section on TSV capacitance, or even a single-TSV capacitor. The *I-V* curve provides the TSV leakage current of the TSV capacitor in the selected voltage range. In case of a TSV array, a high leakage current could be due to all leaky TSVs or to the presence of a single, very leaky TSV in the array; in this case, it is convenient to repeat the leakage measurement on few single TSVs. The *I-V* should cover positive and negative voltages. The voltage of interest is the supply voltage; the corresponding leakage current should not be higher than the sub-threshold current of the transistor technology in the stacked dies served by the TSV connection. Based on experience at IMEC, with an optimized TSV manufacturing process, the expected TSV leakage is in the 1 pA range.
The voltage range can be extended till the breakdown of the TSV insulator, to assess the integrity of the dielectric. For a good quality Si oxide, the expected breakdown voltage should be ~100 V for a 100 nm thick dielectric, by assuming a breakdown hardness of 10 MV/cm for SiO_2; a significantly lower value may indicate lower dielectric thickness in one or more locations, or damaged dielectric.
Fig. 10 illustrates the typical *I-V* curves of a single TSV, before and after annealing, obtained with voltage sweeps covering positive and negative voltages.

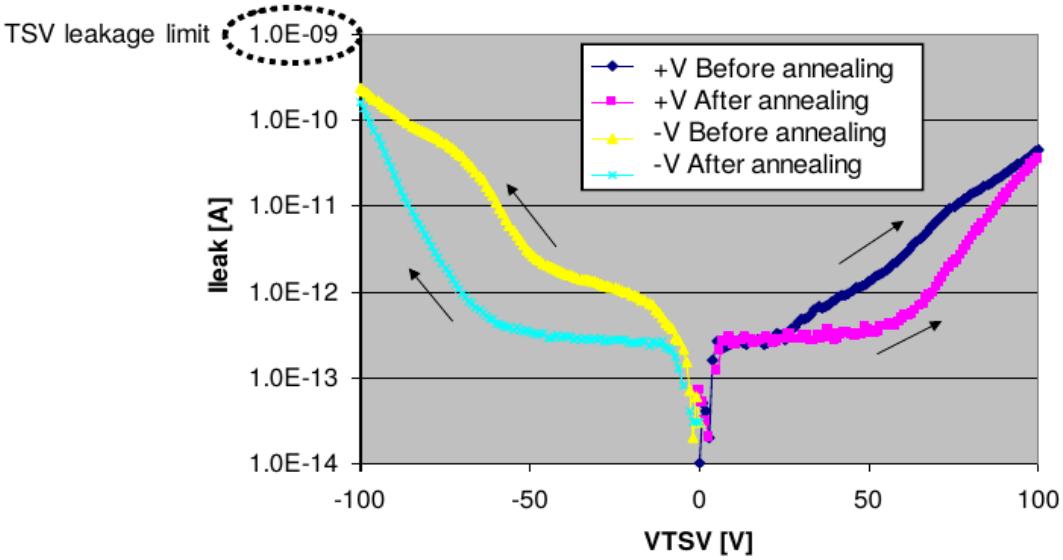


Figure 10: Typical I-V curves of a single TSV, measured up to 100 V*, before and after 100* °C *annealing to release moisture; in all cases, no breakdown occurs and the leakage current is far below 1* nA *at 5* V*, which represents the limit based on the off-state sub-threshold leakage of the CMOS transistors in the dies connected by the measured TSV.*

Measurement of low leakage requires current sensitivity in 10 fA range, especially for single TSV structures. If the *I-V* has to cover the breakdown voltage, the capability to provide a voltage equal or larger than 100 V is an essential requirement.

Summary
The following Table 1 summarizes the guidelines for the four types of measurements proposed.

Table 1: Summary of the guidelines for TSV characterization

Purpose	Measurement	Expected meas.range	Measurement Method	Structure	Desirable meas. capability
TSV characterization	Resistance	10-100 mOhm	4-point resistance on single kelvin TSV	Single Kelvin TSV	Current force=[1-100] mA, Voltage sensitivity: <= 1 uV
	TSV continuity yield	10-100k Ohm	2/4-point resistance on TSV chain	TSV chain	Current force=[1uA-1mA], Voltage sensitivity: <= 1 mV
	Capacitance	1-200 fF	Impedance meas. @10-100 kHz on TSV array	TSV array capacitor	TSV array capacitance > 1pF
	Leakage current	10fA - 1nA @ +/- 5V	2p IV of TSV capacitor array vs. substrate	TSV array capacitor	Current sensitivity: <=10 fA

2.5. DDB reliability of TSV

Time Dependent Dielectric Breakdown (TDDB) testing is widely used for dielectric reliability characterization in gate oxides and BEOL low-*k* dielectric reliability investigations. TDDB measurements may also be needed for TSV liner reliability characterization. However, due to the high aspect ratio of TSVs, the barrier/liner layers inside the TSV have large thickness variations. For example, with an SACVD TEOS/O_3 liner, the TSV liner thickness varies significantly from TSV top to bottom and the position of the weakest link during TDDB tests may not be fixed. Therefore, the lifetime distribution extracted from TDDB testing has a large spread and it is thus difficult to characterize in a reasonable time frame.
An alternative reliability characterization method called "controlled *IV*" (IV_{ctrl}) has been proposed for faster characterization of liner reliability and thus barrier integrity. In this section, both IV_{ctrl} and the traditional TDDB test methods are described and discussed.

TDDB testing
Time dependent dielectric breakdown (TDDB) tests measure the breakdown lifetime under constant voltage stress and are commonly used as a quantitative characterization method for both FEOL gate oxide and BEOL barrier/low-*k* reliability. For a relevant statistical analysis, TDDB measurements are done on large sample sizes and require considerable measurement time and effort. There are several models adopted for dielectric TDDB lifetime prediction; one of the most common is known as *E*-model, which can be expressed by the following equation:

$$t_{bd} \propto \exp(-\gamma E) \tag{1}$$

where t_{bd} is the time to breakdown (failure) and E is the electric field in the dielectric. The factor γ is the field acceleration factor and is an important parameter for characterizing and comparing dielectric reliability of different materials and structures. As shown in the TDDB lifetime plot of Fig. 11, γ is the absolute value of the slope of $\ln(t_{bd})$ vs. E.

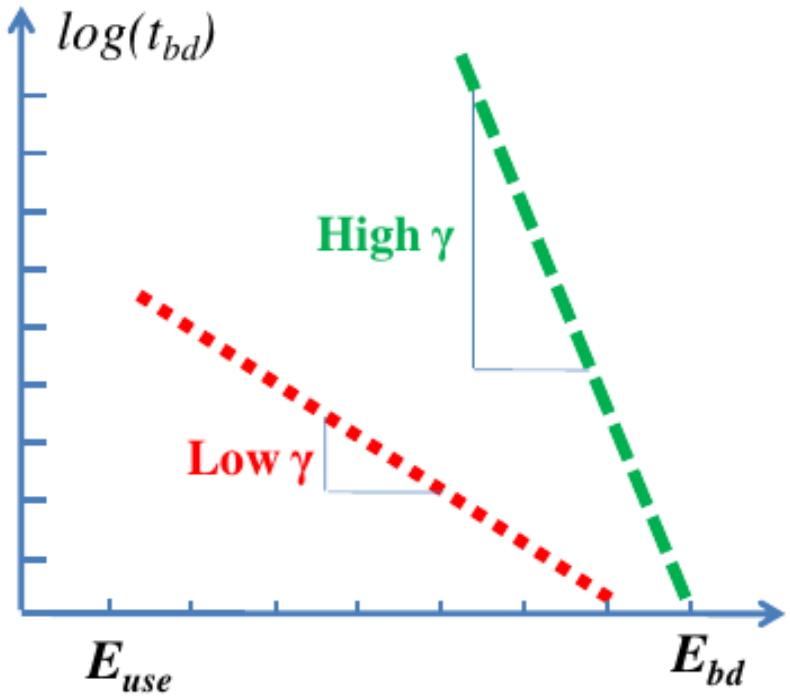


Figure 11: TDDB lifetime plot where the meaning of field acceleration factor γ is demonstrated.

TDDB measurements are done at much higher field than the operating condition, to accelerate the TDDB failure occurrence during the testing. A high field acceleration factor indicates high TDDB lifetime at operating condition and vice versa. γ is typically extracted from TDDB measurements at multiple stress fields.

In a TSV, the trench sidewall is typically very rough, induced by Si deep reactive ion etch (Bosch etch); consequently, the TDDB lifetime distribution at a fixed field results very wide, with many samples with either earlier failure or no failure after a long stress time; obtaining a meaningful TDDB dataset distribution in a reasonable time frame is often impossible. The results of the reliability testing need to be provided timely for a prompt tuning of the integration development; therefore, the availability of an alternative reliability test method which is faster and quantitative is important.

Controlled *IV* theory

Breakdown fields are commonly used for a fast characterization of dielectric film properties and are usually collected from staircase voltage ramp measurements. The voltage ramp rate influences the measured breakdown field since the voltage increments themselves take time and introduce additional TDDB stress. Therefore, the output breakdown field actually contains time information. By assuming the exponential dependency of TDDB lifetime on the stress field described by Equation (1), the equivalent TDDB stress time has been formulated for a certain voltage ramp rate by Berman [3]. For a staircase voltage ramp with the step time interval $\Delta\tau$, the effective stress time t_0 spent at the breakdown field (E_{bd}) can be calculated as [3]

$$t_0 = \Delta\tau \sum_{n=0}^{n=\frac{E_{bd}}{\Delta E}} e^{\gamma(n\Delta E - E_{bd})} = \frac{\Delta\tau}{1 - e^{-\gamma\Delta E}} \qquad (2)$$

where Δh is step field in the voltage ramp measurement and can be calculated from the step voltage ΔV and dielectric thickness S ($\Delta E = \Delta V/S$). For the two breakdown voltage distributions from a dual ramp

rate test, Haase et al. [4] have formulated the relation between the breakdown voltages and the step time intervals as

$$V_{bd}(R_2,i) - V_{bd}(R_1,i) = \frac{S_i}{\gamma}\ln\left(\frac{\Delta\tau_1}{\Delta\tau_2}\right) \quad (3)$$

where $V_{bd}(R_1,i)$ and $V_{bd}(R_2,i)$ are the breakdown voltages for the two ramp rates R_1 and R_2 and i represents a specific fraction of broken-down devices in the two sister distributions. Thus, by doing controlled ramp rate voltage breakdown measurements, the TDDB field acceleration factor γ can be acquired in a much controllable way.

Fig. 12 shows an example of a triple ramp rate test of IV_{ctrl} and the data plot for γ extraction. It must be noted that when the real γ value is very high, the curve in the IV_{ctrl} plot will be quite flat and thus a small perturbation (e.g. charge trapping) will result in a significant slope variation. For such a case, a negative γ value is quite often obtained from reliability experiments. Therefore, generally speaking, a negative γ normally means high reliability and differences between "high γ" and "very high γ" cannot be seen in such cases.

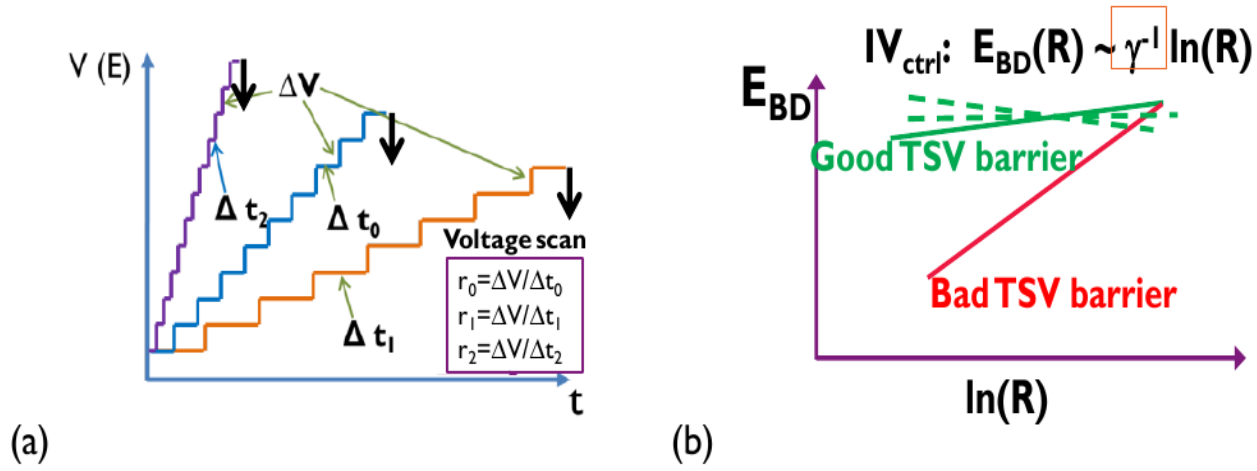


Figure 12: Schematics of controlled IV test and data interpretation: (a) Triple rate controlled IV test with fixed voltage ramp; (b) Breakdown field (voltage) vs. ln(ramp rate) plot for Triple ramp rate IV_{ctrl} for γ value extraction where a negative γ (negative slope) can be present when reliability is good.

Stress modes

For both TDDB and controlled *IV*, two stress modes should be used to characterize separately the barrier integrity and the liner dielectric reliability. As shown in Fig. 13, the Cu driven mode consists of applying a positive bias to the Cu nail with respect to the substrate; the corresponding electric field pushes positive Cu ions away from the Cu nail and causes Cu injection through a defective barrier into the dielectric liner.

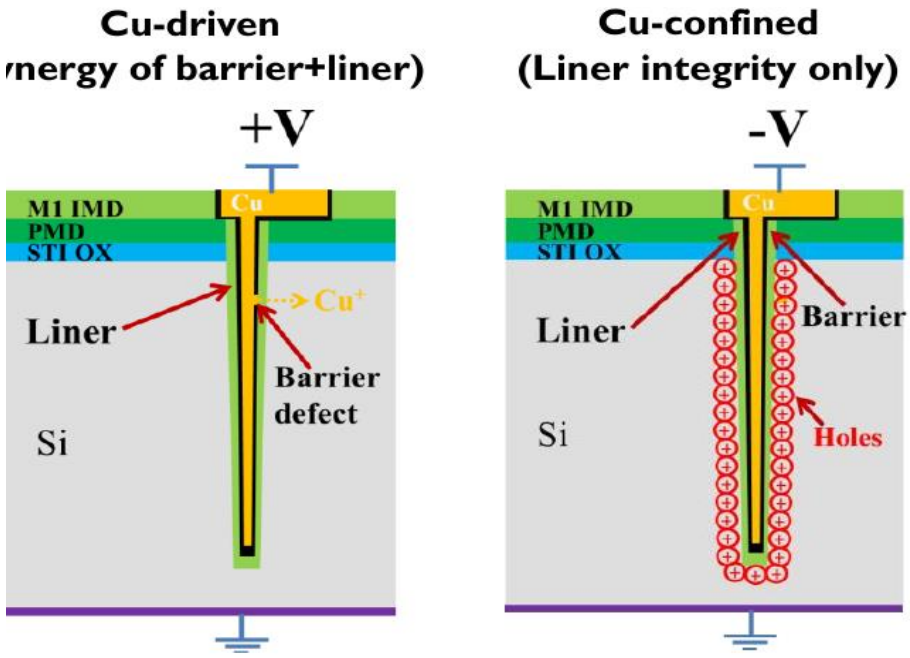


Figure 13: Two stress modes for TSV reliability test: (a) Cu driven mode, where TSV is positively biased and both barrier and liner integrity are tested; (b) Cu confined mode, where TSV is negatively biased and only liner integrity is tested.

In this test mode, both barrier and liner properties are tested: defective barriers or degraded liners will show faster breakdown times. The Cu confined mode consists of applying a negative bias to the Cu nail, thus keeping the Cu ions confined to the nail proximity. No Cu ion can be injected toward the liner, even in presence of a defective barrier; only the liner dielectric integrity is tested. Thus, by combining these two stress modes, it is possible to evaluate separately the liner and barrier contribution to the TSV reliability [5].

Table 2 shows an example of TDDB evaluation results on different liner/barrier combinations that can be used in TSVs, implemented on a planar capacitor structure for a first evaluation of the reliability of the materials. The traditional TDDB and IV_{ctrl} provide consistent values of the field acceleration factor γ for both Cu driven and Cu confined modes. The samples without barrier show low reliability, as expected.

Table 2: Summary of field acceleration factors extracted from IV_{ctrl} and TDDB measurement on different liner/barrier combinations implemented on planar capacitors.

	Liner	Barrier	γ by TDDB (Cu driven) [dec./(MV/cm)]	γ by IV_{ctrl} (Cu driven) [dec./(MV/cm)]
PCAP-1	40nm Liner A	n.a.	1.44	0.72
PCAP-2	40nm Liner A	6nm Barrier A	10.78	11.37
PCAP-3	60nm Liner B (high temp.)	5nm Barrier B	15.4	11.0
PCAP-4	60nm Liner B (low temp.)	5nm Barrier B	11.8	11.2

3. Methods for TSV testing at individual level

3.1. Electrical characteristics

Four point probe method

This is a technique for electrical resistivity measurements at invidivdual TSV level. The technique uses a four-probe setup (see Fig. 14) based on a microscale probe station and a high precision multimeter (HP3458A in four-point measurement mode). A DC current (10 mA) is applied through the probes P1 and P4 and the voltage drop is measured between probes P2 and P3. These two probes P2 and P3 are positioned at different locations on the TSV, from “a” to “e”, as shown in the figure below. The resistivity of each portion is deduced from resistance and dimensions measurements.

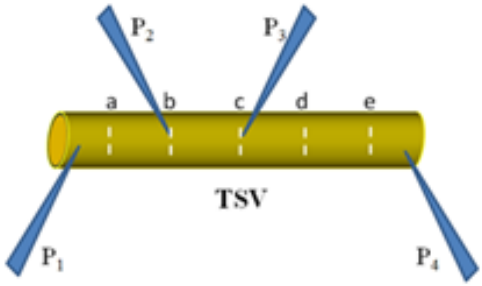


Figure 14: Schematics of four point probe method.

For TSV of small length (*i.e.* 1 mm or less), the **uncertainty** associated to the positioning of the voltage probes (accuracy of 1 µm) mainly due to the limitations of the optical components is the major uncertainty component. This is far larger than the measurement noise and the type B uncertainty components coming from the used high precision multimeter (calibration, drift), the environmental conditions (temperature, pressure relative humidity). For TSV of 120 µm length, the measurement uncertainties amount to 5 % (k = 1).

As an **example of the measured result**, the table below gives the resistivity measured on a TSV of cylindrical geometry, 120 µm long and with a diameter of 10 µm. The voltage measuring probes were positioned at different sections, each of 20 µm long. It can be observed that portions a - b and b - c show significant high resistivity values, which point out the presence of defects in these sections.

TSV section (20 µm)	Resistivity (10^{-8} Ω.m)
a - b	4.01 ± 0.20
b - c	3.51 ± 0.18
c - d	2.09 ± 0.10
d - e	2.06 ± 0.10

Resiscope

As an alternative to four point method, a Scanning Probe Microscopy related technique can be used. The "Resiscope" system is a contact-AFM extension that uses as probe an AFM conductive tip (see Figure 15). A voltage V_{dc} is applied between the tip and the sample and the probe saves changes in current and resistance on a wide range with an external logarithmic amplifier. Thus, two simultaneous information about the sample are obtained: the AFM topography and a mapping of the electrical properties of the sample structure (resistance and current maps). Furthermore, curves of current / voltage can be conducted at various locations on the sample.

The Resiscope system allows the widest dynamics in current or resistance measurement (10 orders of magnitude, from 10^2 Ω to 10^{12} Ω or 100 fA to 1 mA), which allows investigations on a variety of materials (conductive materials, semiconductors or insulators).

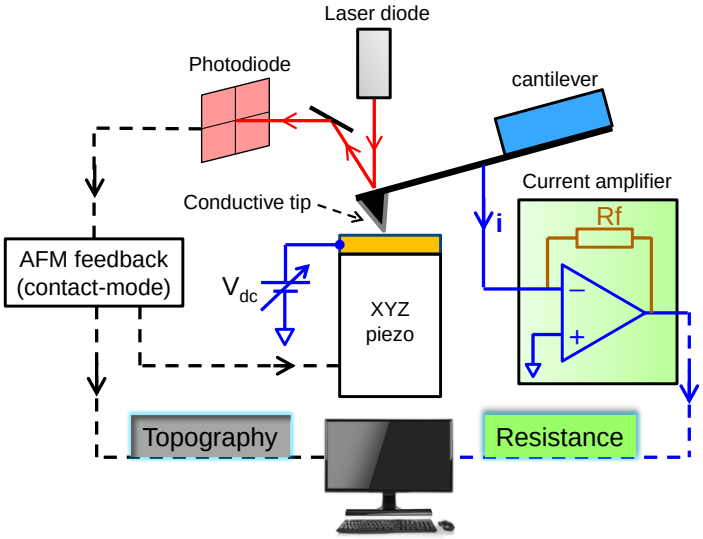


Figure 15: General schematic diagram of a C-AFM.

To date, the resistivity measurement capability using the "Resiscope" system, reach a minimum resistivity value of 0.008 Ω cm, obtained on single phosphorus-doped silicon nanowires [6], which is three orders of magnitude higher than copper resistivity (1.68 x 10^{-6} Ω cm). Unfortunately at this task, we cannot determine a measurement of the copper resistivity because the copper in TSV under study do not reveal an Ohmic behavior.

We conclude that, the Resiscope sytem presents a limitation in the resistivity measurements on metal surfaces.

Resistivity measurements of Cu filled TSV can be determined from resistance measurements with the "Resiscope" system and information about the TSV dimensions. The **uncertainty** is associated, firstly, to the probe-sample contact resistance, which can vary with the contact force during scan of the surface, and consequently affect the total current passing through the nano-contact.

Secondly, the copper stored in the ambient air has a tendency to be oxidized. From the fabrication process, a very fast initial formation of a thin oxide film of about few nm is observed, followed by very slow film growth. Consequently, the probe-sample system might act like a nanoscale Schottky barrier, which can be an unwanted effect during *I/V* measurements.

Also, uncertainty associated to the TSV dimensions should be considered during the determination of the electrical resistivity of copper.

Finally, the probe wear can affect the loss of the conductivity signal, because to slight damage of the apex probe.

For a Cu filled TSV (diameter: 10 µm, length: 120 µm), the theoretical resistance value is 25.7 mΩ , and the Resiscope system is limited to measure resistance values from 10^2 Ω to 10^{12} Ω, with resistance differences as small as 5 Ω could be distinguished.

As an example of the measurement results, Figure 16 shows an optical image of the TSV F (diameter: 10 µm, length: 120 µm, no voids) under study. We have used an Ag paste to assure a good electric contact between the end-TSV and the voltage source. The AFM topography (c) with simultaneous resistance (d) and current (e) maps allow us to distinguish three different regions, which correspond to silicon, copper and a zone A (inside the TSV region). The zone A presents an insulating behaviour, this is probably due to the thick film of copper oxide. As illustrated in figure (e), local *I-V* measurements were performed on Si (in red) and Cu (in blue) using a highly conductive diamond tip. *I-V* spectroscopy on Cu presents a non-Ohmic behaviour, which is due to possible to the copper oxide thin film presents on the copper surface.

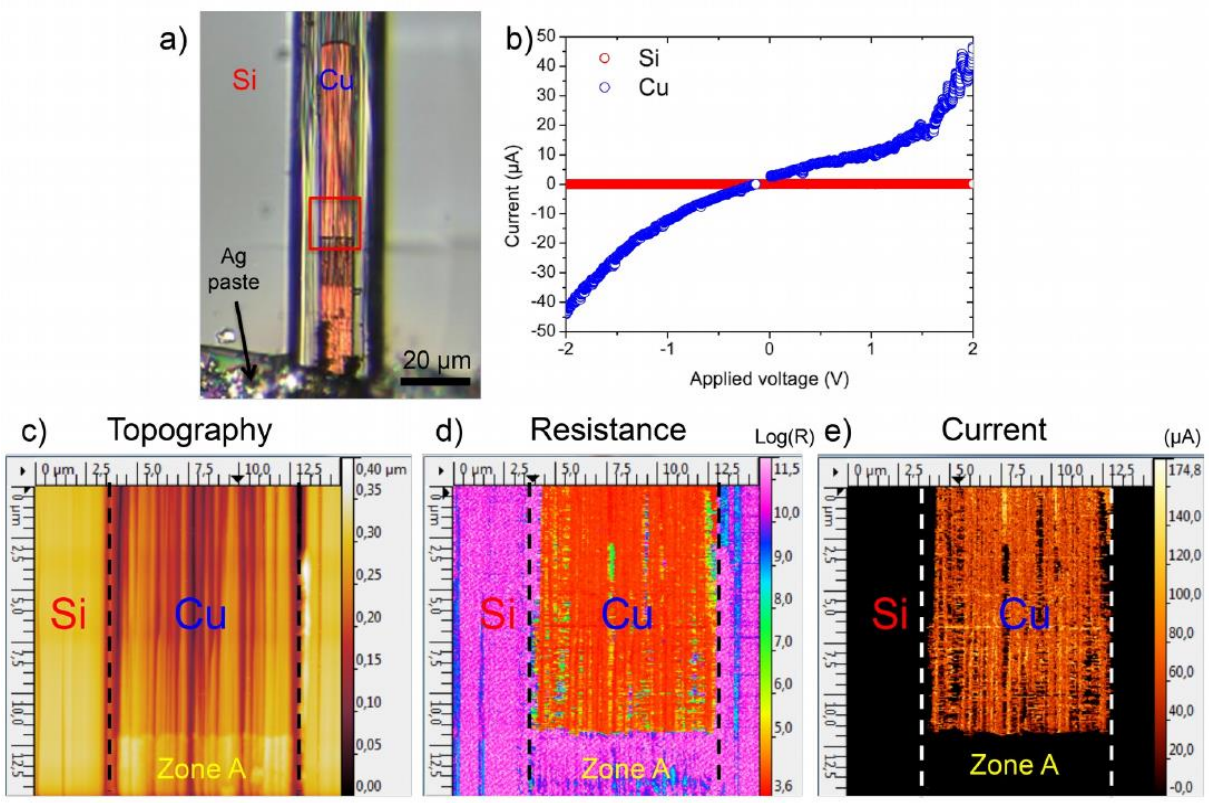


Figure 16. a) Optical image of the CU filled TSV F (10 µm *x 120* µm*, no voids). b) Current-voltage measurements on Cu and Si. AFM Topography (c) and local resistance (d) and current (e) maps illustrating the different electrical properties of the surface. The electrical map was obtained under a bias voltage of 2.5* V*, which is applied to the sample.*

Scanning Microwave Microscope

Another option how to measure electrical resistivity is via a relatively novel technique of Scanning Microwave Microscopy (SMM). The scanning microwave microscope or SMM (at LNE laboratory) consists of an atomic force microscope (AFM) combined with a vector network analyzer (VNA) operating between 0.5 GHz and 6.0 GHz (Figure 17). The VNA is a device that is able to generate and detect microwaves with very high precision and sensitivity in 50 Ω networks and thus serves as generator and detector in the setup. The VNA is connected to the probe via coaxial lines. The SMM is non-destructive to the sample and it is able to simultaneously measure a sample's topography and its (di-)electric properties.
Another SMM setup operating in contact mode is situated at METAS (tuning fork instrument, lateral resolution down to 50 nm, Pt/Ir wire probe with tip radius of 50 nm at its apex, tuning fork leading to probe resonance frequencies of approximately 20 kHz, mechanical excitation controlled with a phase-locked loop). The nanoscale probe in contact with the sample shows very high electric impedances in the kΩ regime which is an unfavorable condition for the VNA being optimized for 50 Ω. To permit for high sensitivity measurements an impedance matching network is introduced between VNA and probe. In case of the system used at METAS, this impedance matching network consists of a bias-tee and a so-called Beatty line (essentially an impedance step - a 50 Ω line with a 25 Ω section in between). The impedance matching circuitry that is used in the system at LNE is sketched in Figure 17. For the electrical part of the SMM measurements, using microwaves with wavelengths in the mm range, this resolution is far from being something obvious to expect. These wavelengths are typical when looking at them in free space and in the far field of a source. However, in the case of a SMM, the microwaves get confined at the probe tip, then acting as source, which furthermore is in contact with the sample of interest. Therefore, the SMM relies on near-field effects when the tip-sample distance is much smaller than the wavelength. Since the tip-size of the SMM is on the order of 100 nm, in the near-field regime thus turns out as the dominating size determining the resolution rather than the wavelength. Another favorable feature of microwaves is their ability to penetrate matter and thus allowing for sub-surface measurements. Operating with fields, the SMM has the advantage of a simple sample preparation. Typically the sample can be scanned as is to take advantage of the sub-surface measurement capabilities. Current based scanning probe methods often demand for extra sample preparation steps as they rely on a back electrode applied to the sample to allow current flows. The microwave penetration depth into the sample of interest is limited by mostly two factors. To a smaller extent the tip size, where the electric field is confined, is a measure for the penetration depth. The main influence however is the so-called skin depth. This skin-depth is a measure of the microwave penetration depth. It depends on the microwave frequency and the material's conductivity and permeability. For example in the case of Cu and at a microwave frequency of 10 GHz the penetration depth is ~650 nm.

SMM combines the nanoscale spatial resolution of the AFM with the broadband electrical measurement capabilities of the VNA. In the SMM reflection mode, a microwave signal is sent directly from the VNA and transmitted through a resonant circuit to a conductive AFM probe that is in contact with a sample being scanned. Depending on the impedance of the tip/sample interface, part of the microwave signal is reflected and measured by the VNA as the scattering S_{11} reflection signal. The ratio of the incident and the reflected signals (the complex S_{11} reflection parameter) gives information on the impedance representing the probe-sample interaction, which is recorded simultaneously with the surface topography.
Resistivity measurements of materials can be extracted from SMM S_{11} reflection measurements. For this purpose, we use an impedance calibration method for nanoscale complex impedance imaging with the SMM, which does not require any calibration samples [7] . In short, tip-sample approach curves are

acquired simultaneously at low kHz frequency (Electrostatic Force Microscopy EFM-mode) and GHz frequency (SMM-mode). The magnitude and phase of the S_{11} parameters and the EFM signals, acquired during tip-sample approach, are used to extract calibrated complex impedance values and to convert measured S_{11} reflection signals into sample capacitance and resistance images.

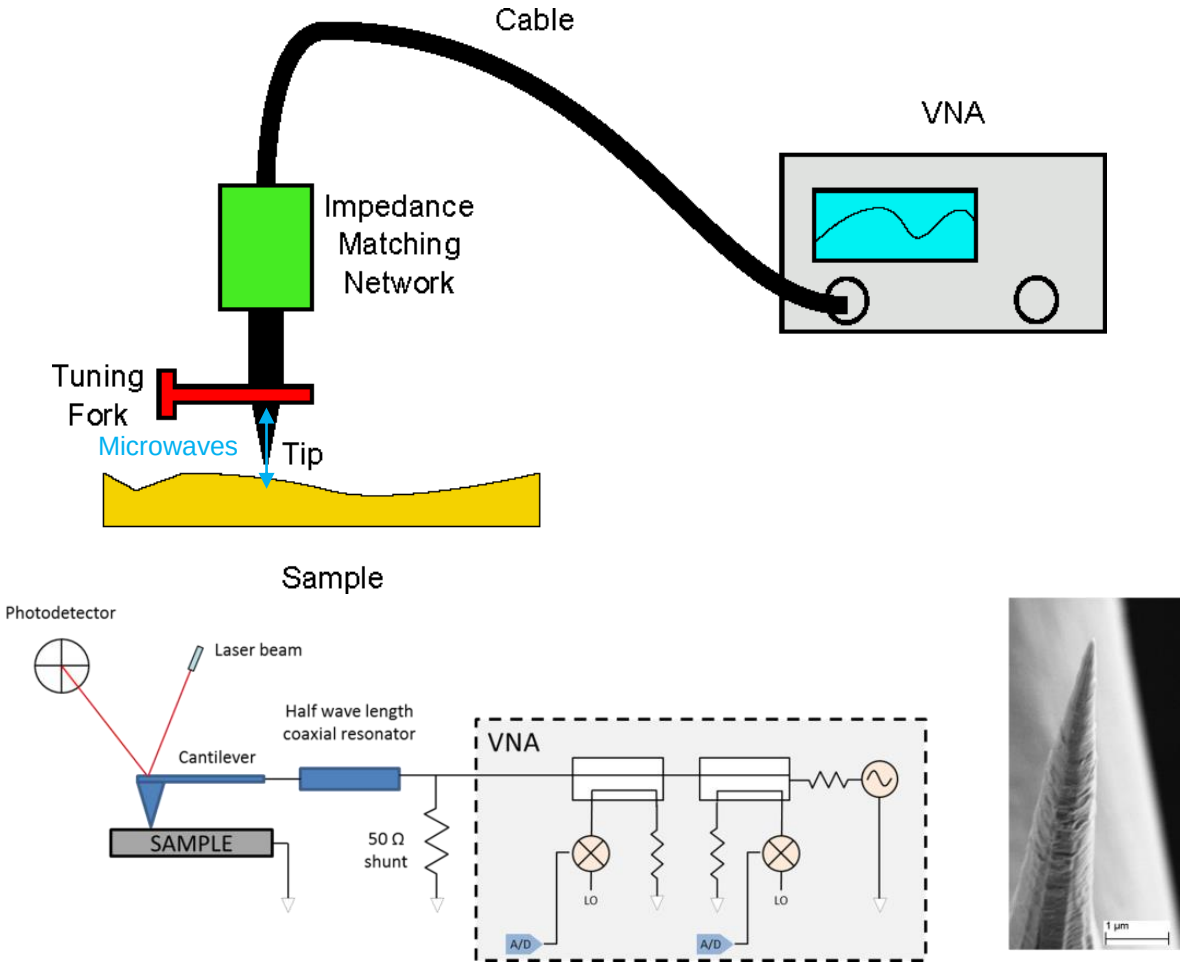


Figure 17 : (bottom left *LNE* and top image /METAS/) General schematic diagram of the SMM microscope and (bottom right image) conductive tip (platinum).

Measurement quantity:

The SMM measures the portion of microwaves that is reflected back from the sample and collected by the tip, this quantity is called the scattering parameter S_{11}. The scattering parameter is a complex quantity consisting of magnitude and phase or imaginary and real part depending on representation. The reflection S_{11} of microwaves is governed by the impedance of the tip-sample interface. Analyzing and modelling this impedance, taking into account sample's material parameters, allows to infer properties of interest of the sample under study.

Recently, resistivity measurements on doped silicon samples with resistivity values ranging from 0.001 Ω cm to 10 Ω cm have been reported [8]. The impedance calibration method to calculate

resistivity from SMM resistance is applied to any semiconductor sample. Unfortunately at this task, we cannot determine a measurement of the copper resistivity because its theoretical value (1.68 x 10^{-6} Ω cm) is outside the range of values allowed by the SMM technique (0.001 Ω cm to 10 Ω cm). Also, resistance differences as small as 20 Ω could be distinguished using the SMM technique, making it difficult to extract the resistance value for a Cu filled TSV (diameter: 10 µm, length: 120 µm), whose theoretical value is 25.7 mΩ.

Regarding **uncertainty** aspects, resistivity measurements of materials are extracted from SMM S_{11} reflection measurements. During scanning of the SMM probe on the sample surface, the probe wear provoked by a slight damage of the apex probe can affect the lateral resolution of SMM, which is limited by the AFM tip apex radii. Then, the uncertainty of the impedance calibration method described above is affected by the approach curve accuracy, the cantilever spring constant, and the geometry of the tip.

Furthermore, the measurement reliability is influenced by the quality of the electrical contact between tip and sample. In case of Cu filled TSV samples, the loss of electrical contact is most likely caused by transient contamination of the copper surface. The copper stored in the ambient air has a tendency to be oxidized, whose oxide thickness increases with aging time.

On the other hand, in contact-mode AFM, the difference between the cantilever deflection signal far from the surface and the setpoint reference is maintained constant during scanning of the surface. However, the cantilever deflection drift of the SMM probe when the tip is far from the surface can affects the tip-sample contact force during scanning and consequently the S_{11} reflection measurements, which varies with the contact force.

As an **example of the measured results**, In Figure 18, the AFM topography (a) of TSV 2 sample (10 µm x 120 µm / No voids) with S_{11}-magnitude (b) and S_{11}-phase (c), allows us to distinguish two different regions, which correspond to the Cu TSV top surface and the silicon substrate. The S_{11}-magnitude and S_{11}-phase maps show an inverted contrast between the copper and silicon surfaces, which indicates the different electrical properties for those materials. However, the extraction of the copper resistivity becomes difficult due to limitation of the SMM technique to obtain resistivity values lower than 0.001 Ω cm. A correct calibration of the SMM instrument would also show a contrast difference in the resistance and capacitance maps, both obtained from conversion of the measured S_{11} reflection signals. However, this calibration step is not possible because the resistivity values that we expect are outside of the range of resistivity values allowed.

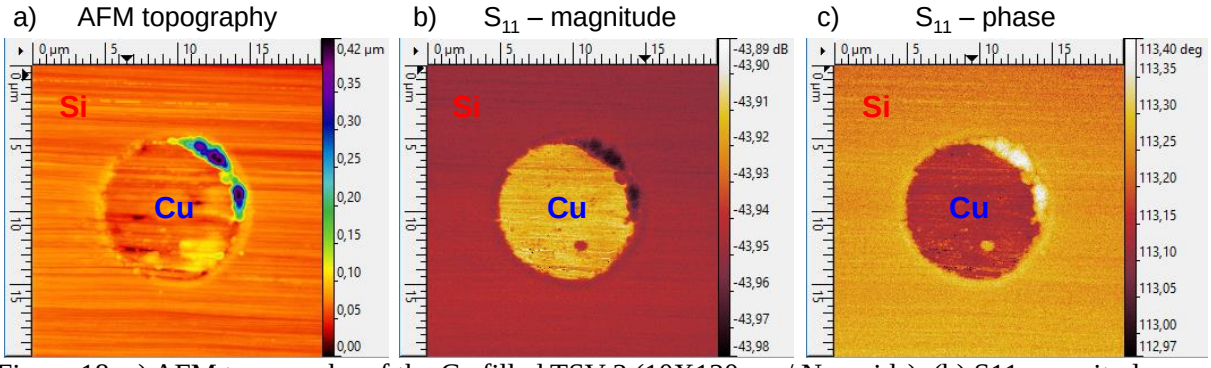


Figure 18: a) AFM topography of the Cu filled TSV 2 (10X120µm / No voids). (b) S11-magnitude. (c) S11-phase. f_{VNA}=2.731 GHz.

3.2. Thermal characteristics

TSV thermal conductivity has two impacts on the performance, it affects the heat spread across the device and if it is locally higher than expected it also creates a local hot spot, increasing the device temperature. Both effects can be addressed using Scanning Thermal Microscopy. SThM belongs to the family of Scanning Probe Microscopy (SPM) techniques, using a sharp probe scanning in contact with the sample surface, obtaining topography and the requested thermal quantity at the same time. All the SThM probes that were used in this study were resistive, so the active element used to measure the local temperature and/or to generate heat is a small resistive element. This can be a thin platinum wire, like in the case of Wollaston wire probes, part of the silicon SPM cantilever with different doping, or microfabricated conductive stripe on the probe.

Local thermal conductivity

To use SThM for local thermal conductivity measurement the probe is heated and the change of the probe resistance due its cooling by sample surface is monitored. As a reference value the probe temperature far from sample is used. Sample is then scanned and both the topography and conductivity contrast signal are stored.

The measurement **uncertainty** in SThM conductivity measurements is mostly related to two effects:

- calibration of the setup: this is typically done via a set of samples with known thermal conductivities and known surface roughness. Due to the probe conductivity limit the method is most sensitive for low conductivity materials (less than approx. 10 W/m/K), and the higher the sample conductivity is the higher is the uncertainty.
- local contact resistance between probe and sample: the contact thermal resistance directly adds to the measured signal, affecting the apparent thermal conductivity. Measurements on rough samples therefore have significantly higher uncertainty.

For samples that are smooth and of small thermal conductivity the uncertainty can be in percents, however for samples like the studied TSVs the uncertainty is extremely high due to the high conductivity. The method is still sensitive to local thermal conductivity variations, however to get the absolute value of conductivity is problematic.

As an **example**, measurements of local thermal conductivity signal on individual TSVs are presented here. The local thermal conductivity affects both the SThM sensitivity and the local temperature distribution, so even if we are interested in local dissipated power, it is an important quantity. In Fig. 19 examples of measurements in the thermal conductivity contrast mode are shown, both for copper covered and uncovered (polished) samples from CEA-LETI. While on polished samples we can see some conductivity contrast at the TSV location and around it, this is not the case of the copper covered sample. In general, the thermal conductivity values of the materials used here (silicon, copper) are not very suitable for SThM measurements as the method is most sensitive for much smaller thermal conductivities. That's the reason why we did not evaluate the local thermal conductivity (the uncertainty would be in tens of percents at least) and we have used the technique only to show the potential defects in TSVs.

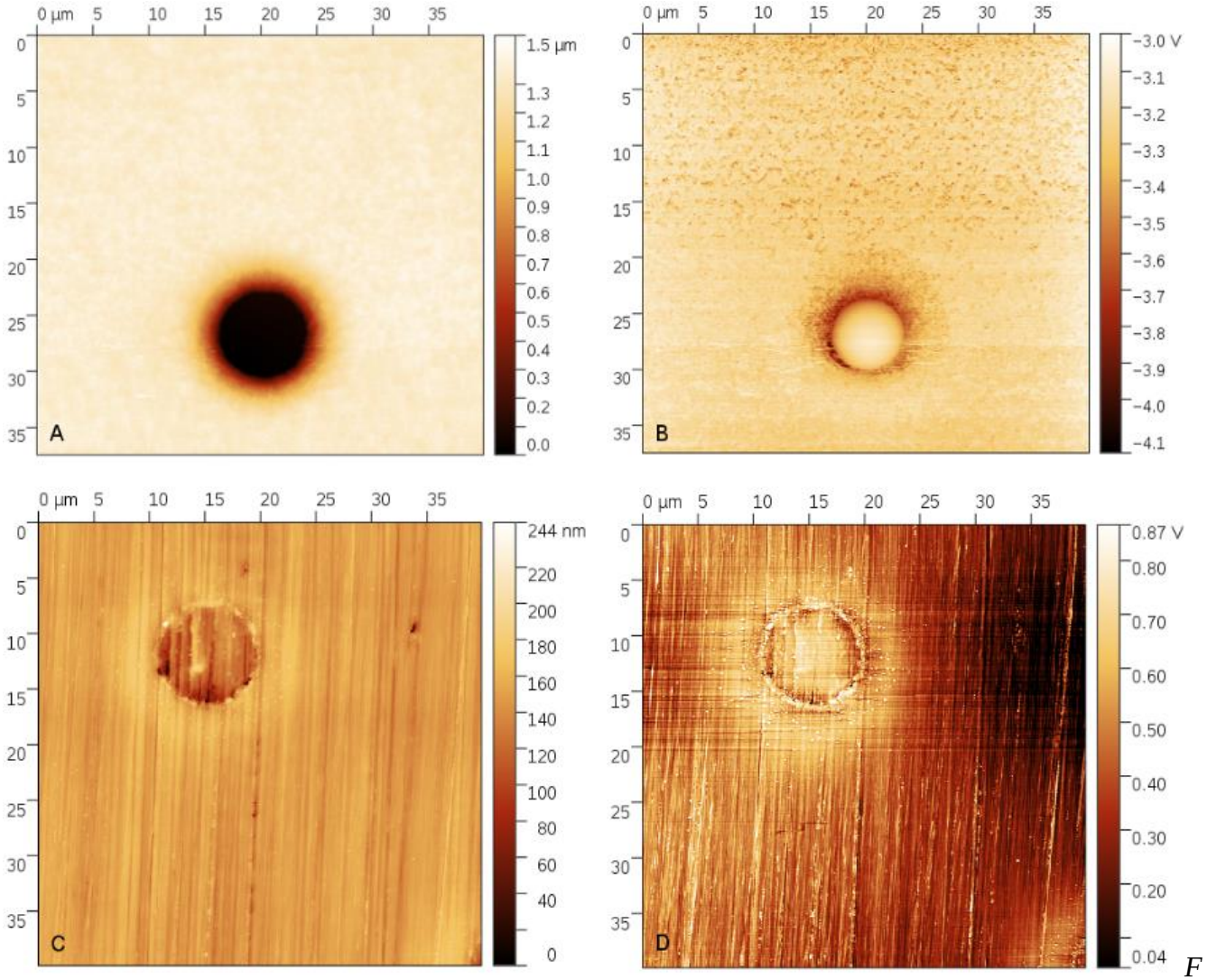


Fig. 19: Local thermal conductivity contrast on TSVs: (A, B) topography and thermal signal on copper coated TSV sample, (C, D) topography and thermal signal on polished TSV sample.

Local temperature variations during operation

If the current sent to SThM probe is small enough the prevent the self-heating, we can observe local temperature of the sample surface. The temperature contrast mode is therefore quite similar to the conductivity contrast (on most of the instruments), except of the probe current. In this way we can monitor the active devices local heatup.

The **uncertainties** related to temperature measurements are again mostly related to probe calibration. Here, the difference of the temperature distribution across the probe while it is calibrated in an oven and while it is scanning over the sample are the biggest uncertainty source. Typical uncertainty for absolute measurements of temperature is few Kelvins, however if only temperature variations are monitored the uncertainty can be significantly lower (tens of miliKelvins for measurements at single spot).

As an **example** of the measurements we show here a large area SPM system result, mapping an active TSV (Fig. 20). Even if the local temperature increase is only in range of miliKelvins it can be observed in the SThM data. As the copper is a good conductor most of the heat is spread across the device and

the local temperature variations are therefore relatively small.

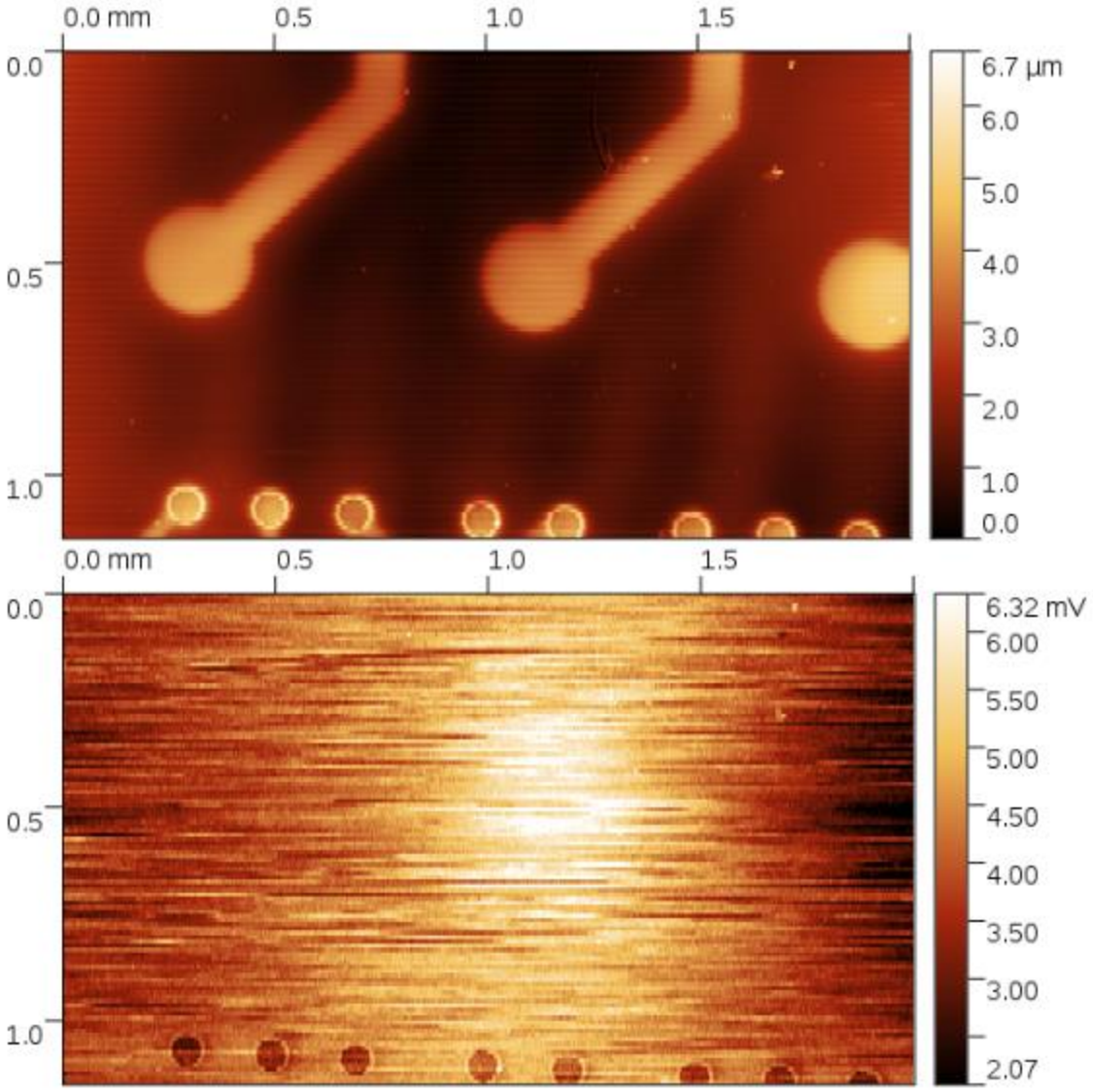


Fig. 20: Topography (top) and local temperature signal (bottom) on an active TSV.

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